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EXAMINER

PAREKH, NITIN

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/775,366

Applicant(s)

JIANG ET AL.

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-52, 108-126, 136-154 and 252-275 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-52, 108-126, 136-154 and 252-269 is/are rejected.
- 7) ☒ Claim(s) 270-275 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

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**DETAILED ACTION**

***Request for Continued Examination***

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/05/03 has been entered. An action on the RCE follows.
2. The amendment filed on 03/27/03 has been entered.

***Specification***

3. Page 11, line 13: Delete "R1, R1 and R3" and insert --- "R1, R2 and R3".

***Claim Objections***

4. Claim 270 is objected to because of the following informalities:  
  
The claim limitations as recited in the claim 270, line 7 should include description/definitions of R1, R2, n and R3.
5. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 271 and 272 have been renumbered 274 and 275.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (US Pat. 6265782).

Regarding claims 1 and 11, Yamamoto et al. disclose an integrated circuit (IC) package comprising:

- a printed wiring board (PWB) substrate (4 in Fig. 4 and 5)
- a die (5 in Fig. 4 and 5)
- an adhesive material (3 and 1 in Fig. 4 and 5 respectively) having a Young's modulus (YM) of about 3 megapascals (Mpa) at a solder reflow temperature (Col. 3, line 34; Col. 7, lines 55-60) attaching the die to the substrate

- the adhesive material comprising a variety of resin/polymer based materials having different compositions/formulations (see examples in Tables 2 and 3; Col. 20-31) which include a component/copolymer and a mixture including a) epoxy, phenol, bisphenol, phenoxy, acrylate copolymer/polyacrylate, methyl acrylate (Col. 4, lines 25-60) having a wide range of molecular weight providing thermosetting properties, and b) polyimide, polyether-imide, etc. (Col. 5, line 55-Col. 6, line 10) providing thermoplastic properties, and
- such compositions/formulations providing a range properties/values to achieve the desired elasticity/modulus, strength, tackiness, surface hardness, and moisture resistance (Col. 20-31).

(Fig. 4 and 5; Col. 3-32).

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2, 9, 12, 13, 108, 118 and 120-122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782).

Regarding claims 2, 108 and 120, Yamamoto et al. teach substantially the entire claimed structure as applied to claim 1 above, except the substrate comprising a ceramic.

Yamamoto et al. further teach a prior art package using conventional substrates such as ceramic to achieve low coefficient of thermal expansion (CTE) and to improve thermal performance (Col. 2, lines 1-13).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the ceramic substrate so that the thermal performance can be improved and the thermal mismatch can be reduced in Yamamoto et al's package.

Regarding claims 9, 12, 13, 118, 121 and 122, Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 above, wherein Yamamoto et al. teach forming different compositions/formulations (see examples in Tables 2 and 3; Col. 20-31) including polymers and mixtures having a wide range of molecular weight, the mixture including acrylate copolymer/polyacrylate and polyimide (Col. 4, lines 25-60; Col. 5, lines 55-60).

10. Claims 3-6 and 110-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) in view of Yew et al. (US Pat. 6049129) and Yamagata (US Pat. 5552637).

Regarding claims 3-6 and 110-114, Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 respectively above, except the die comprising one or more of processor, memory, logic, communication or application specific circuits.

Yew et al. teach an adhesively bonded/encapsulated IC package having IC components including a memory/DRAM and logic circuits (Col. 3, line 40-50).

Yamagata teaches an adhesively bonded IC package/module in a variety of information processing/communication device operations/applications, the package/module having high frequency, high speed and high density/integration memory and central processing unit/processor circuits (Col. 1, lines 35-47; Col. Col. 8, lines 1-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die comprising one or more of memory, processor, logic or application specific//communication circuits as taught by Yew et al. and Yamagata so that the package density, speed and module integration can be improved in Yamamoto et al's package.

11. Claims 7, 8, 10, 14, 15, 115-117, 119, 123 and 124 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) in view of Oxman et al. (US Pat. 6395124).

Regarding claims 7, 8, 10, 116, 117 and 119 Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 above, except the die attach material comprising epoxide, polyepoxide or polyolefin.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising epoxide or polyepoxide as taught by Oxman et al. so that the desired molecular weight and physical properties can be achieved in Yamamoto et al's package.

Regarding claims 7, 8, 116 and 117, forming polyepoxide do not distinguish over Yamamoto et al. and Oxman, because only the final product/structure is relevant, not the process of making such as "forming polyepoxide from epoxide or copolymer or other chemical species". Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marrosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).



Regarding claims 14, 15, 115, 123 and 124, Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 above, wherein Yamamoto et al. teach using compositions/formulations comprising the mixture including polyimide. Yamamoto et al. fail to teach the die attach material comprising a mixture or copolymer of one or more of epoxide, polyepoxide and polyimide.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in a final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising a mixture or copolymer of polyepoxide and polyimide as taught by Oxman et al. so that the desired molecular weight and physical properties can be achieved in Yamamoto et al's package.

12. Claims 16 and 125 are rejected under 35 U.S.C. 103(a) as being unpatentable over the in view of Yamamoto et al. (US Pat. 6265782) in view of Penry (US Pat. 6049094).

Regarding claims 16 and 125, Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 respectively above, except the die attach material having a Shore A hardness of greater than about 70.

Penry teaches using a conventional die attach material having Shore A hardness of about 80 (Col. 4, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a Shore A hardness of greater than about 70 as taught by Penry so that the desired molecular weight and physical properties can be achieved in Yamamoto et al's package.

13. Claims 17, 35, 36, 44, 46-48, 52, 126, 136, 146, 148-150 and 154 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) in view of Narita (US Pat. 6144107).

Regarding claims 17 and 126, Yamamoto et al. teach substantially the entire claimed structure as applied to claims 1 and 108 respectively above, except the die attach material having a Shore D hardness of greater than about 20.

Narita teaches using an IC package having an adhesive resin composition such that the adhesive material has a Shore D hardness between 20-30 to achieve the desired properties/flexibility after curing (Col. 6, line 38).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a Shore D hardness of greater than about 20 as taught by Narita so that the desired flexibility can be achieved in Yamamoto et al's package.

Regarding claims 35, 44, 46-48, 52, 136, 146, 148-150 and 154, Yamamoto et al. disclose an integrated circuit (IC) package comprising:

- a printed wiring board (PWB) substrate (4 in Fig. 4 and 5)
- a die (5 in Fig. 4 and 5) , and
- an adhesive material (3 and 1 in Fig. 4 and 5 respectively) having a Young's modulus (YM) of about 3 megapascals (Mpa) at a solder reflow temperature (Col. 3, line 34; Col. 7, lines 55-60) attaching the die to the substrate

Yamamoto et al. further teach:

I. prior art packages having conventional substrates such as ceramic to achieve low coefficient of thermal expansion (CTE) and to improve thermal performance (Col. 2, lines 1-13), and

II the adhesive material comprising a variety of resin/polymer based materials having different compositions/formulations (see examples in Tables 2 and 3; Col. 20-31) which include a component/copolymer and a mixture including:

- epoxy, phenol, bisphenol, phenoxy, acrylate copolymer/polyacrylate, methyl acrylate (Col. 4, lines 25-60) having a wide range of molecular weight providing thermosetting properties and polyimide, polyether-imide, etc. (Col. 5, line 55- Col. 6, line 10) providing thermoplastic properties
- such compositions/formulations providing a range properties/values to achieve the desired elasticity/modulus, strength, tackiness, surface hardness, and moisture resistance (Col. 20-31).

(Fig. 4 and 5; Col. 3-32).

Yamamoto et al. fail to teach the die attach material being rigid.

Narita teaches using an IC package having a variety of epoxy resin compositions/formulations including an epoxy resin having a hardening agent, the cured resin being rigid having a Shore D hardness around 85 to improve the moisture and crack resistance (Col. 6, line 64- Col. 7, line 5; Col. 5-7).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material being rigid as taught by Narita so that the moisture and crack resistance can be improved in Yamamoto et al's package.

Regarding claim 36, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 35 above, wherein Yamamoto et al. further teach the substrate being a PWB.

14. Claims 18, 26, 28-30, 252, 260, 261 and 263 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129) in view of Yamamoto et al. (US Pat. 6265782) and Satsu et al. (US Pat. 6225418).

Regarding claims 18, 26, 28-30, 252, 260, 261 and 263, Yew et al. disclose an integrated circuit (IC) package comprising:

- a printed wiring board (PWB) substrate (76 in Fig. 3 and 6)
- a die/chip (76 in Fig. 3 and 6)

- an adhesive/resin material (see 90 at the edges of the die and a mid portion between the die and the PWB respectively and 60 in Fig. 3 and 6) attaching the die to the PWB substrate, and
- the die attach adhesive resin comprising a variety of material/thermosetting resin compositions including epoxies, polyimides and silicones (Col. 4, lines 30-55; Col. 7, line 30) having a range properties/values including CTE, elasticity/modulus, strength, etc. (see resin properties in Col. 4 and 7) where CTE ranges from 40-150 ppm/deg. C (see resin properties in Col. 7) to provide reduced failure due to thermal expansion mismatch, thermal shock, cracking and improve adhesion/encapsulation processing (Col. 10, lines 47-60; Col. 6, lines 30-35), the silicone resin having a low CTE of about 40 ppm/deg. C

(Fig. 3 and 6; Col. 3-10).

Yew et al. fail to teach the die attach material having the YM between 0.1 –20 Mpa at solder reflow temperature.

Yamamoto et al. teach an integrated circuit (IC) package having an adhesive material (3 and 1 in Fig. 4 and 5 respectively) having a Young's modulus (YM) of about 3 megapascals (Mpa) at a solder reflow temperature (Col. 3, line 34; Col. 7, lines 55-60) attaching the die to the substrate where the adhesive material further comprises:

- a variety of resin/polymer based materials having different compositions/formulations (see examples in Tables 2 and 3; Col. 20-31) which include a component/copolymer and a mixture including epoxy, phenol,

- 
- bisphenol, phenoxy, acrylate copolymer/polyacrylate, methyl acrylate (Col. 4, lines 25-60) having a wide range of molecular weight providing thermosetting/rigid properties and polyimide, polyether-imide, etc. (Col. 5, line 55- Col. 6, line 10) providing thermoplastic properties, and
- such compositions/formulations providing a range properties/values to achieve the desired elasticity/modulus, strength, tackiness, surface hardness, and moisture resistance ((Fig. 4 and 5; Col. 20-31).

Satsu et al. teach using a variety of die attach/underfill thermosetting resin compositions to achieve the desired heat resistance, crack resistance, modulus and thermal properties (4 in Fig. 2; 8 in Fig. 4A/B; Col. 3-24) in an IC package where the resin compositions/formulations have a range of properties/values including elastic modulus, CTE, adhesive strength, etc. where the CTE has a different range of values, the range being 63-250 ppm/deg. C (see CTE listed in Tables 1-3).

Furthermore, the determination of parameters and respective values/ranges such as YM, hardness, viscosity, thermal expansion coefficient (TEC), etc. of various die attach material/encapsulant and respective composition/formulation in chip packaging/encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, mechanical and electrical properties for the IC package.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a CTE

being less than 400 ppm/deg. C or that between 1-62 ppm/deg. C or 151-400 ppm/deg. C and YM between 0.1 –20 Mpa at solder reflow temperature as taught by Satsu et al. and Yamamoto et al. so that the defects due to cracking, voids and thermal mismatch can be reduced and the adhesion can be improved in Yew et al's package.

15. Claim 109 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) in view of Kunitomo et al. (US Pat. 5550408).

Regarding claim 109, Yamamoto et al. teach substantially the entire claimed structure as applied to claim 108 above, except the substrate comprising a multi-metal layer ceramic.

Kunitomo et al. teach an IC package having a laminated/multi-metal layered ceramic substrate (MLC 11 in Fig. 3; Col. 2, lines 15-25; Col. 9, line 5-45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the multi-metal layer ceramic as taught by Kunitomo et al. so that multilevel routing and electrical performance can be improved in Yamamoto et al's package.

16. Claims 19 and 253 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129), Yamamoto et al. (US Pat. 6265782), and Satsu et al. (US Pat. 6225418) as applied to claims 18 and 252 above, and further in view of APA.

Regarding claims 19 and 253, Yew et al. Yamamoto et al., and Satsu et al. teach substantially the entire claimed structure as applied to claims 18 and 252 respectively above, except the substrate comprising a single metal layer glass-epoxide.

Yamamoto et al. further teach using conventional single or double wiring/metal layer glass-epoxy/polyimide and ceramic substrates (Col. 1, line 25- Col. 2, line 5).

APA teaches using conventional substrates and board made from a glass-epoxide and ceramic (specification pages 1, lines 15-28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate comprising a single metal layer glass-epoxide as taught by Yamamoto et al. and APA so that the rigidity and the thermal mismatch can be reduced in Yew et al. and Satsu et al's package.

17. Claims 20-23 and 254-257 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129), Yamamoto et al. (US Pat. 6265782), and Satsu et al. (US Pat. 6225418) as applied to claims 18 and 252 above, and further in view of Yamagata (US Pat. 5552637).

Regarding claims 20-23 and 254-257, Yamamoto et al., Yew et al. and Satsu et al. teach substantially the entire claimed structure as applied to claims 18 and 252 above, except the die comprising one or more of memory, processor, logic or application specific circuits respectively.

Yew et al. further teach an adhesively bonded/encapsulated IC package having IC components including a memory/DRAM and logic circuits (Col. 3, line 40-50).



Yamagata teaches an adhesively bonded IC package/module in a variety of information processing device operations/applications, the package/module having high speed and high density/integration memory and central processing unit/processor circuits (Col. 1, lines 35-47; Col. 8, lines 1-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die comprising one or more of memory, processor, logic or application specific circuits as taught by Yew et al. and Yamagata so that the package density, speed and module integration can be improved in Satsu et al. and Yamamoto et al's package.

18. Claims 24, 25, 27, 31, 32, 258, 259 and 262 and 264-267 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129), Yamamoto et al. (US Pat. 6265782), and Satsu et al. (US Pat. 6225418) as applied to claims 18, 252 and 261 above, and further in view of Oxman et al. (US Pat. 6395124).

Regarding claims 24, 25, 27, 258, 259 and 262, Yew et al., Yamamoto et al., and Satsu et al. teach substantially the entire claimed structure as applied to claims 18, 252 and 261 above, except the die attach material comprising polyepoxide or polyolefin.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising epoxide or polyepoxide as taught by Oxman et al. so that the desired molecular weight and physical properties can be achieved in Yew et al. and Satsu et al. and Yamamoto et al's package.

Regarding claims 24, 25, 258 and 259, forming polyepoxide do not distinguish over Yew et al., Yamamoto et al. and Satsu et al. and Oxman, because only the final product/structure is relevant, not the process of making such as "forming polyepoxide from epoxide or copolymer or other chemical species". Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marrosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 31, 32 and 264-267, Yew et al., Yamamoto et al., and Satsu et al. teach substantially the entire claimed structure as applied to claims 18 and 261 above, wherein Yamamoto et al. teach using compositions/formulations comprising the mixture including polyimide, except the die attach material comprising a mixture or copolymer of polyepoxide and polyimide.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising a mixture or copolymer of polyepoxide and polyimide as taught by Oxman et al. so that the desired molecular weight and physical properties can be achieved in Yew et al. and Satsu et al. and Yamamoto et al's package.

19. Claims 33 and 268 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129), Yamamoto et al. (US Pat. 6265782), and Satsu et al. (US Pat. 6225418) as applied to claims 18 and 261 respectively above, and further in view Penry (US Pat. 6049094).

Regarding claims 33 and 268, Yew et al., Yamamoto et al., and Satsu et al. teach substantially the entire claimed structure as applied to claims 18 and 261 above, except the die attach material having a Shore A hardness of greater than about 70.

Penry teaches using a conventional die attach material having Shore A hardness of about 80 (Col. 4, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a Shore A hardness of greater than about 70 as taught by Penry so that the desired molecular weight and physical properties can be achieved in Yew et al., Satsu et al. and Yamamoto et al's package.

20. Claims 34 and 269 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yew et al. (US Pat. 6049129), Yamamoto et al. (US Pat. 6265782), and Satsu et al. (US Pat. 6225418) as applied to claims 18 and 261 respectively above, and further in view of Narita (US Pat. 6144107).

Regarding claims 34 and 269, Yew et al., Yamamoto et al., and Satsu et al. teach substantially the entire claimed structure as applied to claims 18 and 261 above, except the die attach material having a Shore D hardness of greater than about 20.

Narita teaches using an IC package having an adhesive resin composition such that the adhesive material has a Shore D hardness between 20-30 to achieve the desired properties/flexibility after curing (Col. 6, line 38).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a Shore D hardness of greater than about 20 as taught by Narita so that the desired flexibility can be achieved in Yew et al., Satsu et al. and Yamamoto et al's package.

21. Claims 37-41 and 139-142 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) and Narita (US Pat. 6144107) as applied to claims 35 and 136 respectively above, and further in view of Yew et al. (US Pat. 6049129) and Yamagata (US Pat. 5552637).

Regarding claims 37-41 and 139-142, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 35 above, except the die comprising one or more of communication, memory, processor, logic or application specific circuits respectively.

Yew et al. further teach an adhesively bonded/encapsulated IC package having IC components including a memory/DRAM and logic circuits (Col. 3, line 40-50).

Yamagata teaches an adhesively bonded IC package/module in a variety of information processing/communication device operations/applications, the package/module having high frequency, high speed and high density/integration memory and central processing unit/processor circuits (Col. 1, lines 35-47; Col. 8, lines 1-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die comprising one or more of communication, memory, processor, logic or application specific circuits as taught by Yew et al. and Yamagata so that the package density, speed and module integration can be improved in Narita and Yamamoto et al's package.

22. Claims 42, 43, 45, 49, 50, 143, 144, 145, 147, 151 and 152 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) and Narita (US Pat. 6144107) as applied to claims 35 and 136 above, and further in view of Oxman et al. (US Pat. 6395124).

Regarding claims 42, 43, 45, 144, 145 and 147, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 35 above, except the die attach material comprising polyepoxide or polyolefin.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising epoxide or polyepoxide as taught by Oxman et al. so that the desired molecular weight and physical properties can be achieved in Narita and Yamamoto et al's package.

Regarding claims 42 and 43, forming polyepoxide do not distinguish over Yamamoto et al. and Narita, because only the final product/structure is relevant, not the process of making such as "forming polyepoxide from epoxide or copolymer or other chemical species". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also

In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 49, 50, 143, 151 and 152, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claims 35 and 136 above, wherein Yamamoto et al. teach using compositions/formulations comprising the mixture including polyimide, except the die attach material comprising a mixture or copolymer of polyepoxide and polyimide.

Oxman et al. teach an adhesively bonded IC package having epoxy resin compositions/formulations comprising epoxides including diepoxides, polyepoxides (Col. 11, line 43; Col. 11-13) monoolefins, diolefins and polyolefins (Col. 11, line 10; Col. 2, line 47) to achieve the desired physical properties in final cured composition

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material comprising a mixture or copolymer of polyepoxide and polyimide as taught by Oxman et al. so that the desired

molecular weight and physical properties can be achieved in Narita and Yamamoto et al's package.

23. Claims 51 and 153 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) and Narita (US Pat. 6144107) as applied to claims 35 and 136 respectively above, and further in view of Penry (US Pat. 6049094).

Regarding claims 51 and 153, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 35 above, except the die attach material having a Shore A hardness of greater than about 70.

Penry teaches using a conventional die attach material having Shore A hardness of about 80 (Col. 4, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die attach material composition having a Shore A hardness of greater than about 70 as taught by Penry so that the desired molecular weight and physical properties can be achieved in Narita and Yamamoto et al's package.

24. Claims 137 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) and Narita (US Pat. 6144107) as applied to claim 136 above, and further in view of Kunitomo et al. (US Pat. 5550408).



Regarding claim 137, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 136 above, except the substrate comprising a multi-metal layer ceramic.

Kunitomo et al. teach an IC package having a laminated/multi-metal layered ceramic (MLC 11 in Fig. 3; Col. 2, lines 15-25; Col. 9, line 5-45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the multi-metal layer ceramic as taught by Kunitomo et al. so that multilevel routing and electrical performance can be improved in Narita and Yamamoto et al's package.

25. Claim 138 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US Pat. 6265782) and Narita (US Pat. 6144107) as applied to claim 136 above, and further in view of APA.

Regarding claim 138, Yamamoto et al. and Narita teach substantially the entire claimed structure as applied to claim 136 above, except the die comprising a germanium.

APA teaches the die comprising a germanium material (specification page 1, line 18).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the die comprising the germanium as taught by APA so that the package density, speed and module integration can be improved in Narita and Yamamoto et al's package.

***Response to Arguments***

26. Applicant's arguments filed on 05-05-03 have been fully considered but they are not persuasive.

Applicant contends that Yamamoto et al. teach the Young's modulus (YM) being in the range 3-50 Mpa and not the value between 0.1 to 20 Mpa.

However, the YM of about 3 Mpa or any value between 3-20 Mpa is between the range 0.1 to 20 Mpa. Similarly, the CTE value between 40-150 ppm/deg. C and 63-250 ppm/deg. C as taught by Yew et al. and Satsu et al. respectively, meet the requirement of CTE being less than 400 ppm/deg. C or that between 1-62 ppm/deg. C or 151-400 ppm/deg. C as recited in claims 18, 252 and 261 respectively.

***Allowable Subject Matter***

27. Claim 270 would be allowable if rewritten or amended to overcome the objections set forth in this Office action.

28. Claims 271-275 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

29. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for the allowance of claims 270-275 is the inclusion of the limitations of an integrated circuit (IC) package having a die being attached to a

substrate using a polyimide die attach material where the polyimide has a Young's modulus (YM) between 0.1 to 20 Mpa and the polyimide is a compound having a chemical formula:  $(R1-CO-NH-CO-R2)_n-R3$  such that R1, R2 and R3 are  $(C_1-C_{24})$ alkenyl,  $(C_2-C_{24})$ alknyl and  $(C_1-C_{24})$ alknyl respectively. The prior art references Yamamoto et al. (US Pat. 6265782), Narita (US Pat. 6144107) Kunitomo et al. (US Pat. 5550408), Yew et al. (US Pat. 6049129), Satsu et al., Yamagata (US Pat. 5552637), Oxman et al. (US Pat. 6395124) and Penry (US Pat. 6049094) lack the teachings of the polyimide die attach material having the YM between 0.1 to 20 Mpa and the polyimide compound having the chemical formula as recited in claims 270-275.

### ***Conclusion***

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-F are cited as being related to polyimide based die-attach adhesives.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Art Unit: 2811

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

NP  
07-12-03

*Nitin Parekh*  
Nitin Parekh

PATENT EXAMINER  
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